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600 °C Logic Gates Using Silicon Carbide JFET's

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Introduction

Complex electronics and sensors are increasingly being relied on to enhance the capabilities and efficiency of modern jet aircraft. Some of these electronics and sensors monitor and control vital engine components and aerosurfaces that operate at high temperatures above 300 °C. However, since today's silicon-based electronics technology cannot function at such high temperatures, these electronics must reside in environmentally controlled areas. This necessitates either the use of long wire runs between sheltered electronics and hot-area sensors and controls, or the fuel cooling of electronics and sensors located in high-temperature areas. Both of these low-temperature-electronics approaches suffer from serious drawbacks in terms of increased weight, decreased fuel efficiency, and reduction of aircraft reliability. A family of high-temperature electronics and sensors that could function in hot areas would enable substantial aircraft performance gains. Especially since, in the future, some turbine-engine electronics may need to function at temperatures as high as 600 °C.

This paper reports the fabrication and demonstration of the first semiconductor digital logic gates ever to function at 600 °C. Key obstacles blocking the realization of useful 600 °C turbine engine integrated sensor and control electronics are outlined.

Technology Selection

Silicon carbide (SiC) presently appears to be the strongest candidate semiconductor for implementing 500-600 °C integrated electronics in the nearer term, as competing high temperature electronics technologies are either physically incapable of functioning at this high of a temperature range (silicon and silicon-on-insulator), or are significantly less-developed (GaN, diamond, etc.) than silicon carbide. Discrete silicon carbide devices such as pn junction diodes, junction field effect transistors (JFET's), and metal-oxide-semiconductor field effect transistors (MOSFET's) have previously demonstrated excellent electrical functionality at 600 °C for relatively short time periods [1]. However, for such electronics to be useful in crucial turbine-engine applications, much longer 600 °C harsh-environment lifetimes must eventually be realized. Between 500 to 5000 hours of operation is needed for various jet engine ground tests, while many years of reliable operation is required for insertion into everyday passenger aircraft.

The operational lifetime of SiC-based transistors at 600 °C is not limited by the semiconductor itself, but is instead largely governed by the reliability and stability of various interfaces with the SiC crystal surface. The physical degradation of the metal-semiconductor ohmic contact interface limits the 600 °C operating lifetime of all devices, while high temperature MOSFET operating lifetime is also limited by the electrical integrity of the oxide-semiconductor. While silicon electronics experience clearly demonstrates that complementary MOSFET (CMOS) technology is desired for implementing integrated circuits, development of the necessary high electrical quality gate-insulators capable of long-term 600 °C operation will likely prove elusive for many years to come [2]. Thus, junction-based transistors without gate insulators appear more feasible in the nearer term, especially given recent progress toward improving the 600 °C high temperature durability of SiC ohmic contacts [3]. Of the candidate junction-based transistor technologies that might be used to implement SiC integrated circuits, the pn junction gate JFET seems closest to demonstrating long-term operation at 600 °C. Prototype SiC bipolar transistors demonstrated to date have exhibited low current gains insufficient for practical use in complex integrated circuits, while the Schottky barrier gates employed in SiC metal-semiconductor field effect transistors (MESFET's) allow too much undesired gate-to-channel leakage at 600 °C [4].

The basic current-voltage properties of SiC JFET's at 600 °C are qualitatively similar to room-temperature GaAs MESFET's employed in high-speed digital IC's. Therefore, a resistive load direct-coupled FET logic (DCFL) approach, with some obvious parallels to high-yield GaAs DCFL, was adopted to demonstrate simple 600 °C digital logic using SiC JFET's. A simple inverter logic gate merely requires a near-zero threshold voltage FET coupled to a resistor.

The non-planar epitaxial gate JFET design shown in Figure 1 was adopted in favor of a planar ion-implanted structure, largely to alleviate the challenging process of sufficiently activating high-dose p^+ ion implants in SiC. The two-level interconnect approach uses oxidation-resistant silicon nitride as the dielectric passivant along with oxidation resistant gold for the metal interconnect. Contrary to the depiction of Figure 1, the devices are laid out so that both the second and third layers of silicon nitride always covered the first via layer to the oxygen-sensitive metal-SiC ohmic contact interface. However, because non-optimized ohmic contact metals were employed in this experiment, long term 600 °C operation was not obtained.

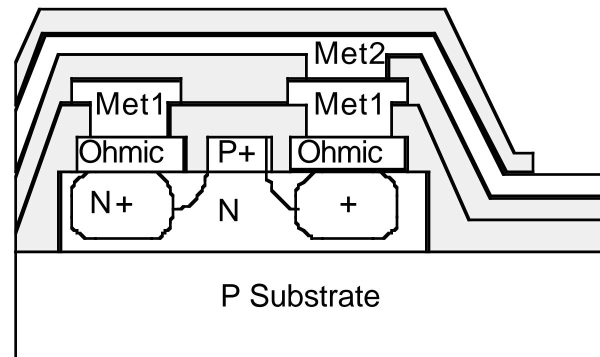

Figure 1: Simplified (see text) cross-sectional representation of 6H-SiC epitaxial JFET's used to implement 600 °C logic gates. The shaded regions are insulating silicon nitride dielectric.

Fabrication Process

The mesa-isolated epitaxial channel JFET structure shown in Figure 1 was grown (starting from an off-axis commercial p-type 6H-SiC substrate [5]) at the NASA Glenn Research Center using the epitaxial growth system described in [6]. Proper application of site-competition dopant control principles was key to successfully realizing this device structure [7]. An underlying p^- buffer epilayer around 12 microns thick and doped p-type below 5×10^{15} cm^{-3} is not depicted in Figure 1. A 0.5 – 0.7 µm n-channel layer doped around 1×10^{16} cm^{-3} was grown to obtain threshold voltages acceptably close to zero over the temperature range of interest. The thin p^+ gate epilayer (0.1 - 0.2 µm, $N_A > 10^{20}$ cm^{-3}) must be as degenerately doped as possible, to assure sufficient electrical contact to the gate layer as well as adequate conductivity through long narrow gate fingers with no metal directly on top. Site-competition enables all the key n-type and p-type layers to be grown within a single continuous run that minimizes undesired contamination and dopant spikes that can arise from growth interruption and re-initiation [8]. It also enables better immunity to epi-reactor impurities that can harm reproducibility as the reactor components, especially the sample-holding susceptor, can degrade from one growth run to the next.

Following epitaxial growth, an aluminum p^+ gate pattern etch mask is defined and patterned by liftoff. A reactive ion etch (RIE) in 14 CHF_3 : 10 O_2 400 W plasma removes the p^+ epilayer from unmasked areas to expose the n-channel layer. Without removing the first gate etch mask, a second aluminum etch mask defining mesas for the active n-channel areas is deposited and liftoff patterned. A second RIE to a depth of approximately 0.7 µm is then carried out to isolate each device. Both aluminum etch masks are then stripped with a wet etch.

In preparation for ion implantation, approximately 0.1 µm of silicon is E-beam deposited over the entire wafer. Then, a 0.8 µm layer of silicon is liftoff patterned to delineate areas for high dose nitrogen source/drain implants to facilitate ohmic contacts to the n-channel layer. The wafers are then sent to a commercial vendor [9] for 600 °C nitrogen implantation of a box profile using 1.4×10^{15}, 7×10^{14}, and 3.6×10^{14} cm^{-2} doses at 80, 40, and 20 keV energies, respectively. Following ion implantation the silicon mask layers are chemically stripped in 1 HF : 1 HNO_3. The same basic implant process is then repeated to carry out lighter-dose nitrogen implant (3.2×10^{12}, 8×10^{11}, 1.2×10^{12}, and 1×10^{12} cm^{-2} dose at 33, 24, 18, and 10 keV, respectively) that self-aligns with the etched p^+ gate as shown in Figure 1. This second implant prevents complete pinchoff of the n-layer resistors by the sub-channel and surface depletion regions and increases transistor source-to-gate and gate-to-drain conductance. After implant mask stripping and solvent/acid wafer cleaning, the nitrogen implants are electrically activated by placing the wafer into a closed SiC crucible (made from SiC wafer pieces) and annealing at 1400 °C for 30 minutes in an argon atmosphere tube furnace. The wafer is again cleaned with acids to remove any residual oxides that might have formed during the implant anneal.

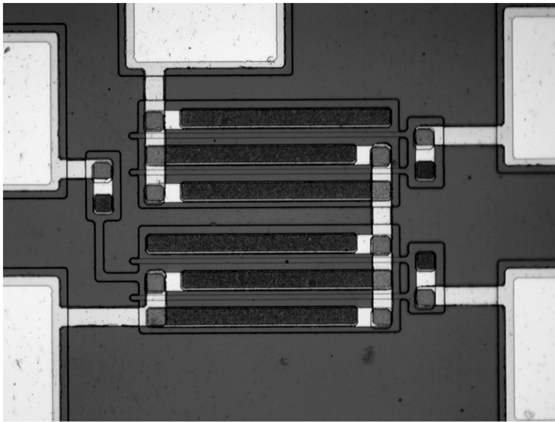

Figure 2: Optical micrograph of 6H-SiC JFET NAND gate prior to 600 ℃ testing. The logical output is the bottom left bondpad, while the input pads are along the right side. The positive (V_{DD}) and negative (V_{SS}) power supply pads are on the top left and top middle, respectively. Each bondpad is 100 x 100 μm, and each of the four gate fingers is 3 x 150 μm.

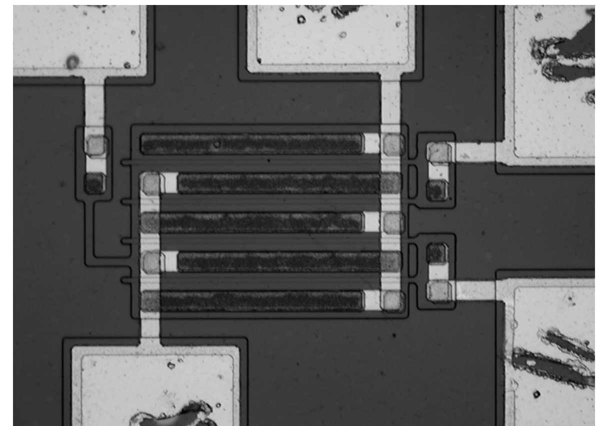

Figure 3: Optical micrograph of 6H-SiC JFET NOR gate following 600 °C electrical testing. The bottom left bondpad is the output, while the input pads are along the right side. The positive (V_{DD}) and negative (V_{SS}) power supply pads are on the top left and middle. Each bondpad is 100 x 100 μm, and each of the four gate fingers is 3 X 150 μm.

A 0.3 μm thick layer of gold (E-beam deposited, patterned by liftoff) formed the contacts to both the n^+ source/drain implant regions as well as the p^+ gates. At this stage of the process, the basic electrical functionality of the JFET's and resistors was verified at room temperature on a probing station.

A first layer of silicon nitride passivation was sputter deposited to a thickness of around 0.3 – 0.4 μm. The deposition of this layer was broken into two segments to minimize chances of undesired pinhole defects spanning the complete thickness of the layer. Patterned vias through the first nitride layer was then dry etched in a 5 CHF_3 : 0.4 O_2 150 W plasma using photoresist as the etch mask. 0.3 μm thick gold interconnects were then liftoff patterned on top of the nitride. The same basic nitride/via/metal process was then repeated for a second level of gold interconnect. A third and final nitride deposition and bondbad via etch completed the circuit fabrication process. The completed NAND and NOR gates are shown in the optical micrographs of Figures 2 and 3.

Electrical Testing

All circuit testing was carried out in air under low-light conditions using a probing station with the sample sitting on a customized temperature-controlled heating element. Gold-coated tungsten probe tips were employed to minimize probe degradation by oxidation during high temperature testing.

Figures 4 and 5 show the functional waveforms collected from the NAND and NOR gates at 300 ℃, respectively. Figures 6 and 7 show operation of the same gates at 600 ℃. As indicated by the supply voltages given in each figure caption, adjustment of the substrate bias ($V_{substrate}$) and power supply bias (V_{DD}) was necessary to compensate for current-voltage property changes with temperature, as the circuit noise margins were not sufficient to absorb these changes while maintaining basic functionality. Therefore, these circuits are not capable of operation over the desired 25 ℃ to 600 ℃ temperature range using fixed power supply voltages. High temperature degradation of both the probe-tips and the ohmic contacts limited operational circuit testing at 600 ℃ to less than one hour. The Figure 3 device picture taken following 600 ℃ testing shows visible evidence of contact degradation compared to the Figure 2 device photo taken prior to high temperature testing.

Discussion

While the work described here does represent a first for high temperature integrated circuit operation, it also illustrates areas where additional technology development is necessary before 600 ℃ SiC-based circuits can become useful. The operational lifetime of the circuit at 600 ℃ could be extended by using separately optimized n-type and p-type ohmic contacts specifically designed to resist high-temperature degradation. However, it will be difficult to measure this improvement on a probing station where the probe tips themselves are degrading. Therefore, the parallel development of 500 – 600 ℃ packaging is very important to further development of the chip-level technology. The ability to thermally cycle packaged devices under electrical bias would also aid the observation of longer term electrical instabilities like

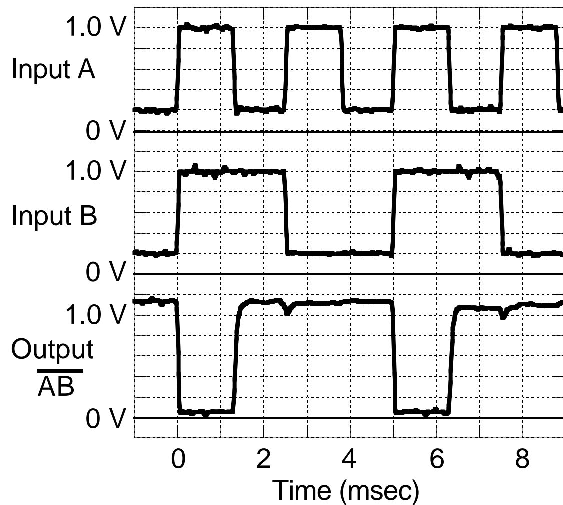

Figure 4: NAND gate test waveforms at 300 °C with V_{DD} = 2.1 V, V_{SS} = 0 V, $V_{substrate}$ = 0 V.

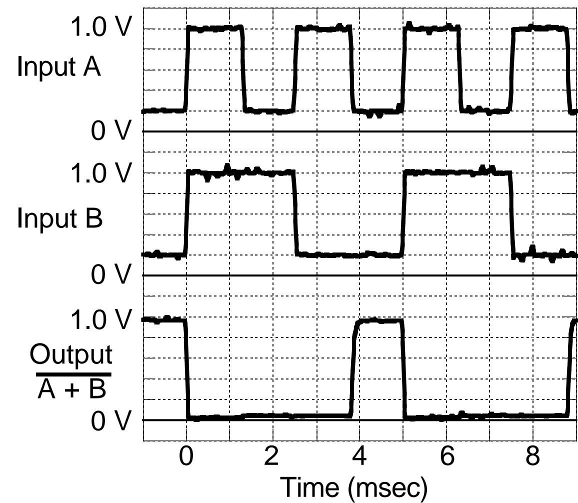

Figure 5: NOR gate test waveforms at 300 °C with V_{DD} = 3.5 V, V_{SS} = 0 V, $V_{substrate}$ = 0 V.

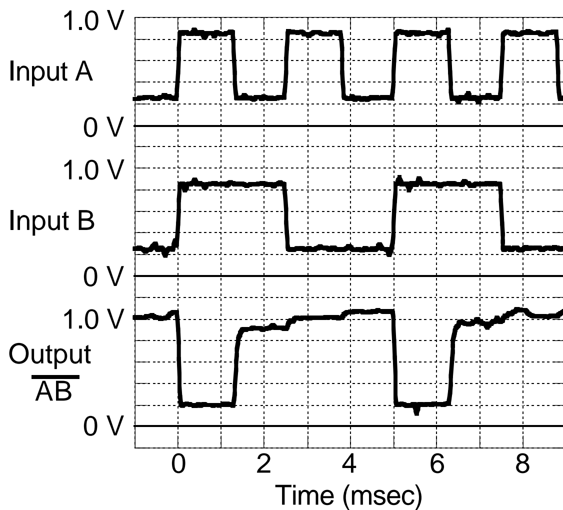

Figure 6: NAND gate test waveforms at 600 °C with V_{DD} = 2.5 V, V_{SS} = 0 V, $V_{substrate}$ = -1.4 V.

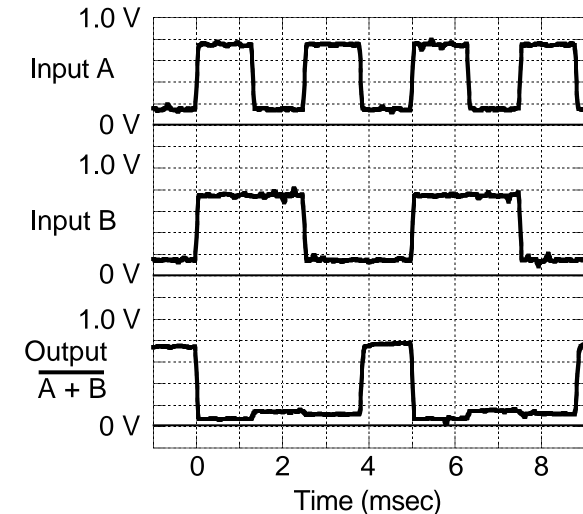

Figure 7: NOR gate test waveforms at 600 °C with V_{DD} = 3.5 V, V_{SS} = 0 V, $V_{substrate}$ = -1.8 V.

those shown to limit the operating lifetime and usefulness of 300 °C operational amplifier circuits based on SiC doped-channel MOSFET's [10]. Effective elimination of such instabilities, if present in integrated circuit compatible SiC JFET's, will be necessary before 500 - 600 °C integrated circuits implemented in this technology can become useful.

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