

Current-Voltage Testing of Candidate Dielectric Materials for 500 °C SiC Integrated Circuits

Carl W. Chang
ASRC Aerospace
NASA Glenn Research Center
21000 Brookpark Road, M.S. 77-1
Cleveland, OH, 44135 USA
Phone: 1-216-433-5495
FAX: 1-216-433-8643
Carl.W.Chang@nasa.gov

Philip G. Neudeck
Glenn M. Beheim
David J. Spry
NASA Glenn Research Center
21000 Brookpark Road, M.S. 77-1
Cleveland, OH 44135 USA
Phone: 1-216-433-8902
FAX: 1-216-433-8643
Neudeck@nasa.gov

Abstract

High temperature operation (500 °C and higher) of integrated circuits offers important benefits to harsh environment applications such as aerospace, aeronautics, and energy production. SiC-based electronics are a promising solution to this need for high temperature operation. However, thermally activated degradation of materials used in conjunction with SiC (such as interconnect metals and insulators) are a limiting factor in the long-term operation of SiC integrated circuits. In particular, dielectric material properties degrade with increased operating temperature but are nevertheless critical in the ability to demonstrate long-term integrated circuits with multiple layers of interconnect. We fabricated and tested capacitors using several different dielectric thin films to initially compare their potential suitability for use in high temperature (500 °C and above) SiC integrated circuit applications. We conducted current versus voltage testing (up to hundreds of volts) at 25, 300, and 500 °C on capacitors made from reactively sputtered silicon nitride, silicon nitride deposited by plasma enhanced chemical vapor deposition (PECVD), silicon dioxide deposited from tetra-ethyl-ortho-silicate (TEOS) by PECVD, and amorphous SiC deposited by ion-beam assisted sputtering. The I-V characteristics of the 0.7- μm -thick amorphous-SiC capacitors were unacceptably leaky ($> 0.6 \text{ A/cm}^2$ at 0.4 MV/cm at room temperature). As-deposited 0.7- μm -thick PECVD TEOS silicon dioxide (deposited at 400 °C) demonstrated the best insulating performance with a leakage current density of less than $1 \mu\text{A/cm}^2$ for an electric field of 0.7 MV/cm (50 V) at 500 °C. These initial I-V measurements at elevated temperatures will be used to down-select dielectrics for prolonged electrical stress testing at 500 °C.

I. Introduction

High temperature operation of electronics at 500 °C and above is an enabling technology for a variety of applications in aerospace, automotive, energy production, and other industries [1, 2]. A key aspect of high temperature electronic operation is the stability and reliability of insulating materials used in the fabrication and packaging of these circuits. High temperature SiC integrated circuits have very recently demonstrated long-term 500 °C operation [3-6]. These integrated circuits (ICs) used a layer of silicon nitride to insulate the metal interconnect layer from the SiC substrate. The ICs demonstrated were basic digital gates and amplifiers. More complicated SiC integrated circuits for high temperature operation will consist of far more transistors and require multiple layers of metal interconnect and dielectric. Furthermore, many ICs will also require on-chip

capacitors. Therefore, proper choice of dielectric will be critical for further development of high temperature integrated circuits.

The dielectric utilized in these high temperature ICs must perform reliably at extreme temperatures. A dielectric for application in high temperature ICs must meet the requirement of sufficient breakdown strength and lifetime at these elevated temperatures. Even at voltages well below breakdown, leakage current through the dielectric at elevated temperatures is a significant concern and must be sufficiently suppressed by the dielectric.

There are a number of dielectric films that were considered for this application. In order to determine which of these films would satisfy the application requirements we examined a number of oxide and nitride dielectrics.

These films were compared via evaluation of test capacitors fabricated using each of the films under consideration. These test capacitors were evaluated at both room and elevated temperatures to characterize the dielectric films. The results of these experimental findings will be used to down-select the number of films that we will consider for use and consequently subject to prolonged electrical stress testing at 500 °C.

II. Experimental

A. Test Capacitors

Test capacitors were fabricated on silicon wafers using the various dielectrics. First, a three-layer stack of 1000 Å titanium (Ti), 4000 Å tantalum silicide (TaSi₂), and 2000 Å platinum (Pt) was sputter deposited on each bare silicon wafer for use as the bottom electrode [7]. This metal stack is the high temperature contact used in the prototype SiC ICs [3-6]. Each dielectric was then deposited on a wafer. Electron-beam evaporation of 1000 Å titanium and then 2000 Å gold (Au) was used to deposit the top electrode for the test capacitors. The top metal was patterned using a lift-off process. Circular test capacitors with diameters of 110, 120, or 160 μm were evaluated. The dielectrics were all nominally 7000 Å thick.

The deposition methods for the dielectrics were limited due to the presence of the bottom contact metals. Although the bottom contact metal stack was designed for high temperature operation [7], most foundries and cleanroom laboratories do not permit a metal coated wafer in a MOS-clean high temperature, low pressure chemical vapor deposition (LPCVD) furnace. Therefore, alternative methods of depositing oxides and nitride were utilized. The dielectrics and their deposition techniques are detailed below.

B. Dielectric Materials

The dielectrics tested during this initial evaluation consisted of the following: amorphous silicon carbide, silicon dioxide, and silicon nitride.

The amorphous silicon carbide (a-SiC) was deposited by ion-beam assisted sputtering. These films were deposited by the U.C. Berkeley Microlab [8]. The a-SiC film was originally developed for use as an encapsulating film for microelectromechanical systems (MEMS) and not optimized for use as a dielectric insulator. Silicon dioxide (SiO₂) was deposited by plasma enhanced chemical vapor deposition (PECVD) using tetra-ethyl-ortho-silicate (TEOS) precursor. These silicon dioxide films were deposited at two temperatures, 350 and 400 °C, through the MEMS and Nanotechnology Exchange foundry [9]. The silicon nitride films were deposited by two methods, by PECVD at 350 °C and by pulse DC reactive sputtering. The PECVD nitride was obtained through the MEMS and Nanotechnology Exchange foundry while the pulse DC reactive

sputtered nitride was deposited in the NASA Glenn Microfabrication laboratory.

C. Measurement Setup

Ramped voltage testing was used to determine the leakage current and breakdown voltage/field for each dielectric. Ramped voltage testing is a rapid and efficient method to determine the performance of dielectrics [10]. The voltage was ramped while the current was recorded using a source measure unit. These characterizations were carried out on an automated probe station with an insulated, thermally controlled chuck. Each dielectric was characterized at room temperature, 300 °C, and 500 °C while exposed to normal laboratory atmosphere. A current limit was placed on the source measure unit to prevent damage to the probe and/or test sample.

D. Minimum Breakdown Field

The designed peak operating voltage for our first generation SiC transistors is 50 V. Therefore, at the minimum a dielectric should be capable of a breakdown field of 0.7 MV/cm at elevated temperature for the 7000 Å dielectric thickness under consideration. Should a dielectric exhibit large leakage current or not be capable of the required breakdown field, the dielectric would be eliminated from further long-term testing.

III. Results and Discussion

A. Amorphous Silicon Carbide

Figure 1 plots the room temperature results of current density (J_d) versus applied electric field (E) for a-SiC deposited by ion-beam assisted sputtering.

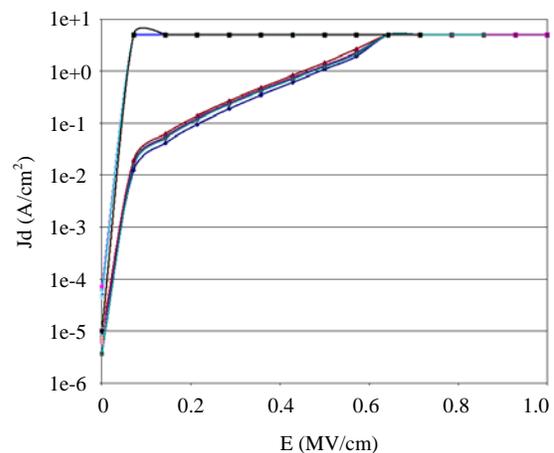


Figure 1. Current density versus applied electric field for a-SiC at room temperature (20 devices plotted).

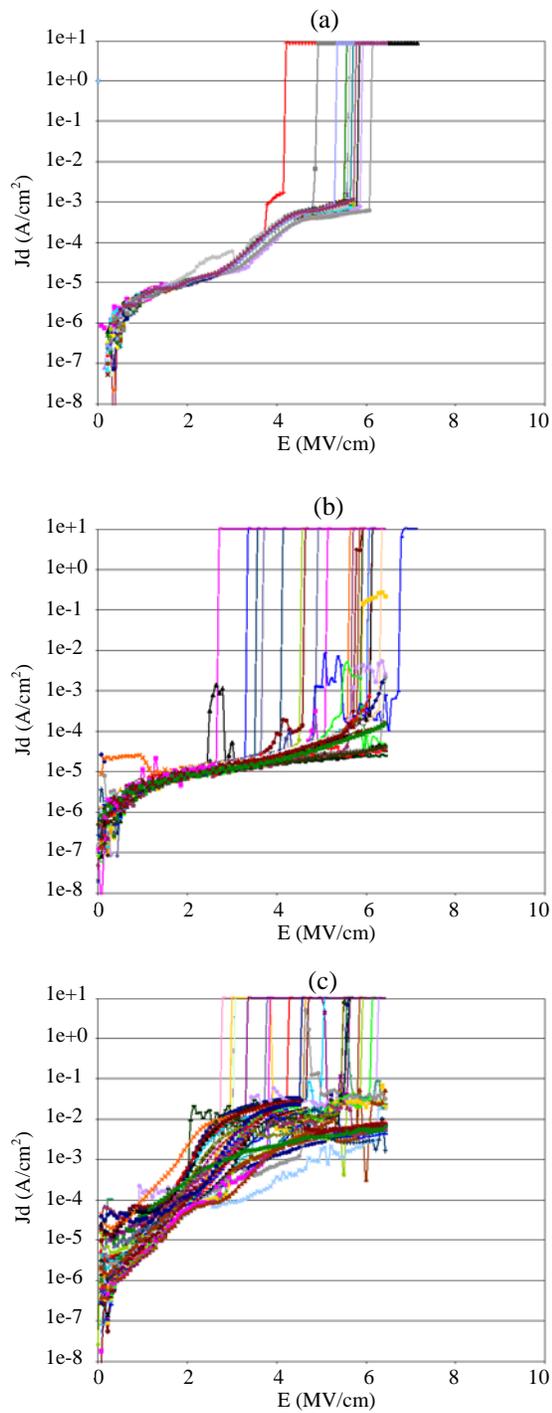


Figure 2. Current density versus applied electric field for 350 °C PECVD TEOS at (a) 25 °C (47 devices shown), (b) 300 °C (41 devices shown), and (c) 500 °C (44 devices shown).

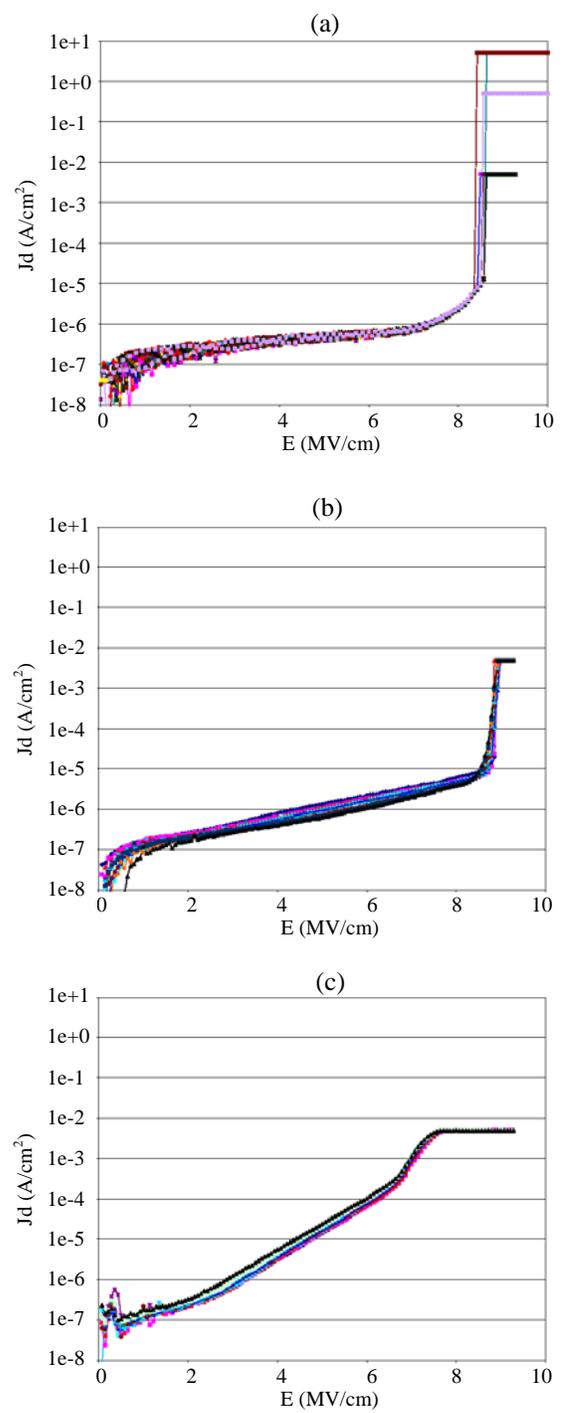


Figure 3. Current density versus applied electric field for 400 °C PECVD TEOS at (a) 25 °C (15 devices shown), (b) 300 °C (12 devices shown), and (c) 500 °C (12 devices shown).

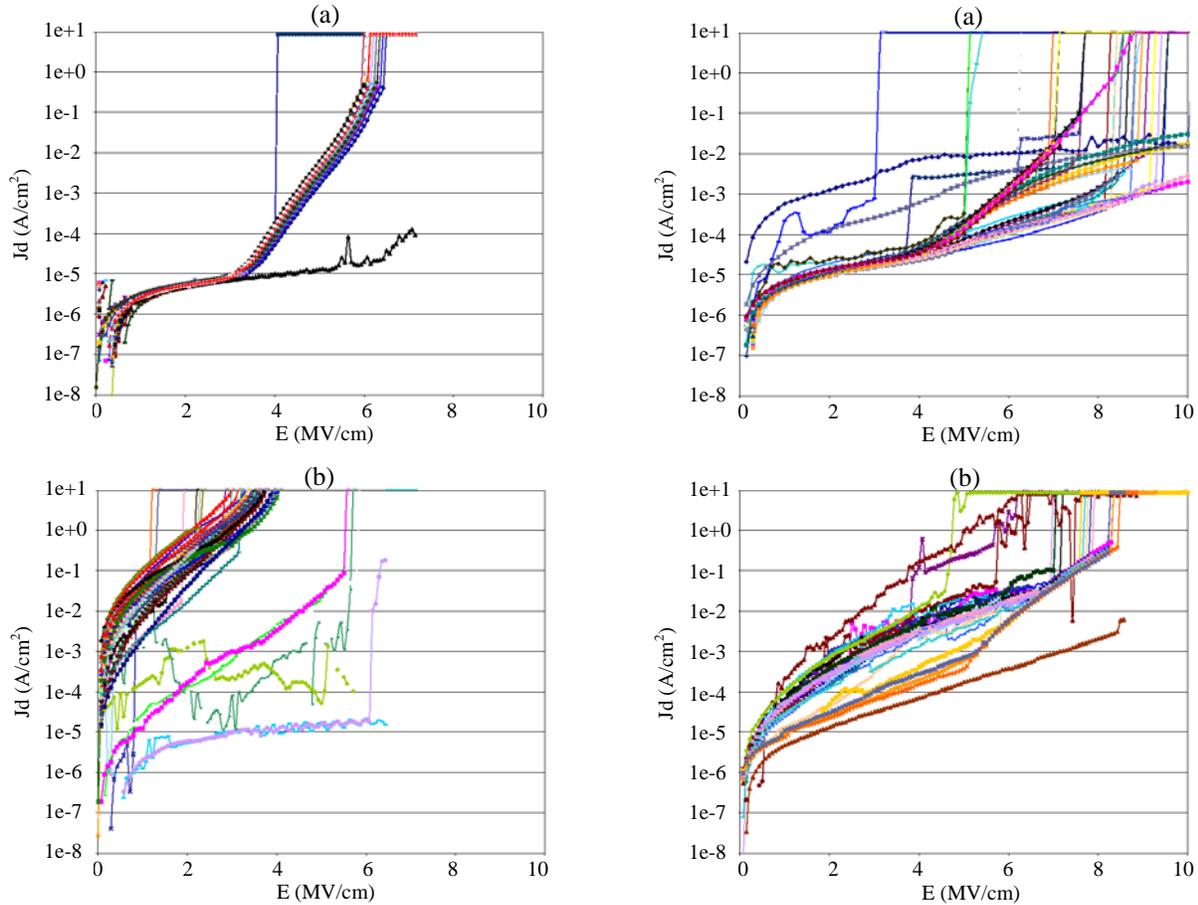


Figure 4. Current density versus applied electric field for PECVD Si_3N_4 at (a) 25 °C (34 devices shown) and (b) 300 °C (46 devices shown).

The capacitors were circular with a diameter of 160 μm . Results show a large leakage current density through the dielectric, even for low electric fields at room temperature. These capacitors reached the compliance set in the source-measure unit (5 A/cm^2) typically below an applied field of 0.7 MV/cm (50 V). Due to the high current leakage that occurred at room temperature, further testing at 300 and 500 °C was not conducted. Amorphous SiC was therefore eliminated from further testing or consideration.

B. PECVD TEOS Silicon Dioxide 350 °C

The results of testing PECVD TEOS silicon dioxide deposited at 350 °C are shown in Figure 2. The capacitors were circular with 120 μm diameter for room temperature and 110 μm diameter for 300 and 500 °C. Current leakage measured below 0.7 MV/cm was found to be near the noise floor of the test setup for all three temperatures.

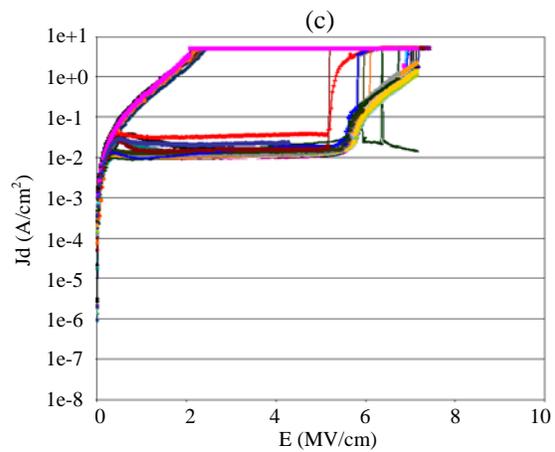


Figure 5. Current density versus applied electric field for reactively sputtered Si_3N_4 at (a) 25 °C (39 devices shown), (b) 300 °C (23 devices shown), and (c) 500 °C (39 devices shown).

The average breakdown field at room temperature is 5.6 MV/cm, with a standard deviation of 0.24 MV/cm. At 300 °C the average breakdown field is 5.4 MV/cm with a standard deviation of 1.07 MV/cm for the devices that exhibited breakdown. It should be noted that 14 of the 41 devices tested did not reach breakdown before the maximum applied voltage of 450 V (6.4 MV/cm). At 500 °C the average breakdown field was 4.7 MV/cm with a standard deviation of 1.07 MV/cm. As was similarly observed for the devices tested at 300 °C, half of the devices tested at 500 °C did not reach breakdown before the maximum applied voltage of 450 V (6.4 MV/cm). Breakdown fields observed at both 300 and 500 °C had a fairly wide spread, however they were no lower than 2.7 MV/cm for any of the devices tested at either of these temperatures.

C. PECVD TEOS Silicon Dioxide 400 °C

Ramped voltage results for PECVD TEOS silicon dioxide deposited at 400 °C are shown in Figure 3. The capacitors tested were circular with a 160 μm diameter. At room temperature and 300 °C, the leakage current measured was within the noise level of the experimental setup until breakdown occurred. The breakdown field at room temperature was 8.6 MV/cm on average, with a standard deviation of 0.07 MV/cm. At 500 °C the leakage gradually increased with increasing voltage until the compliance current set in the source measure unit was reached. No breakdown was observed at 500 °C, for fields up to approximately 7.7 MV/cm.

D. PECVD Silicon Nitride 350 °C

Test capacitor results at room temperature and 300 °C are shown in Figure 4. The results of testing at room temperature on circular capacitors with a 120 μm diameter indicate the PECVD silicon nitride performs reasonably well, with an average breakdown field of 6.1 MV/cm and a standard deviation of 0.39 MV/cm. At 300 °C the results on 110- μm -diameter capacitors indicate that the film allows too much leakage current. This high leakage can be seen in Figure 4b. Further test results at 500 °C confirm that the film is no longer capable of behaving as an insulator, as current flows for most of the tested devices almost immediately when a voltage is applied. Therefore, as-deposited PECVD silicon nitride does not appear to be a viable candidate for further long-term testing.

E. Reactively Sputtered Silicon Nitride

Figure 5 summarizes the results of testing reactively sputtered silicon nitride capacitors. The diameters of the capacitors tested were 110 μm at room temperature, 120 μm at 300 °C, and 160 μm at 500 °C. At room temperature the average breakdown

field was 8.1 MV/cm but with a large standard deviation of 1.46 MV/cm. The data at 300 °C had a very large spread in leakage current prior to breakdown. At 500 °C the test capacitors exhibited two distinct behaviors. The devices either leaked continuously and reached the current compliance set in the source measure unit around 2 MV/cm, or the devices exhibited a lower leakage rate until approximately 5.7 MV/cm, at which point current leakage would then begin to increase until either current compliance was reached or breakdown occurred. The average breakdown field for the devices with this latter behavior was 6.7 MV/cm with a standard deviation of 1.02 MV/cm. For those devices that leaked significantly upon application of electric field, most reached a leakage current density of 1 A/cm² at less than 1.7 MV/cm. The sputtered silicon nitride did not appear to perform as well as the PECVD TEOS silicon dioxide. Nevertheless, the sputtered silicon nitride performed adequately as the insulator in single-level-interconnect SiC JFET ICs that have successfully operated for thousands of hours at 500 °C [3-6]. The transistor results indicated that there is an improvement in insulating performance following an annealing, or burn-in, period [4].

F. Discussion

Insulator performance can be somewhat predicted from theory using ideal band structure and current transport equations. In practice, however, measured charge transport and breakdown of experimental insulators often is dominated by non-ideal properties of the film, often related to the physical processing that created the dielectric. For example, we observed a significant difference between the leakage properties of silicon nitride dielectric formed by PECVD versus reactive sputtering processing.

The results of our initial testing indicate that some of the studied dielectric films may be good candidates for use in our next generation of high temperature SiC ICs, and thus for further testing. The results also indicate which dielectrics might not be good candidates for high temperature IC use and can be eliminated from further consideration.

The a-SiC film, deposited using a non-optimized process, can be eliminated from further testing due to its high rate of leakage current that was observed at room temperature. Although PECVD Si₃N₄ behaved fairly well at room temperature, its behavior at 300 °C was poor and only worsened at 500 °C. Therefore, it appears that PECVD Si₃N₄ can also be removed as a possible candidate for further long-term testing.

The remaining three films are PECVD TEOS SiO₂ deposited at 350 and 400 °C, and reactively sputtered Si₃N₄. The reactively sputtered Si₃N₄ has been utilized, in a

thicker form (1.1 μm), in our present single-level-interconnect SiC ICs and has been found to be adequate for use in the present application following a burn-in time at 500 °C [4]. The results of the test capacitor testing bear this out as the dielectric does not break down at 0.7 MV/cm at 500 °C. However, the thickness of the 1.1 μm Si_3N_4 film will present challenges for use in a multilayer interconnect scheme. In addition, further work is required to investigate the effects that anneal time and temperature may have on the performance and reliability of the silicon nitride film. The two PECVD TEOS silicon dioxide films appear to offer improved leakage and breakdown performance over the silicon nitride presently utilized. Both silicon dioxide films demonstrated lower leakage current density at elevated temperatures when compared to the reactively sputtered silicon nitride (although all films generally exhibited increased pre-breakdown leakage current at higher temperatures). The PECVD TEOS silicon dioxide deposited at 400 °C, especially, looks promising as a possible dielectric for use at 500 °C. These three films will be considered for further testing, both ramped and long-duration constant voltage tests at high temperatures.

Future testing of these candidate materials will involve thinner dielectrics to increase the measurable leakage current. The present dielectric thickness of 7000 Å is too thick to be able to measure the leakage current at low electric field levels. Often in the present measurements, the low field leakage current is within the measurement noise floor. Furthermore, a thinner dielectric will decrease the voltage required to break down the test capacitor. Presently when the dielectric does break down there is damage to surrounding devices. Future devices will utilize a high temperature top metal contact, which will enable us to investigate annealing effects. We also will seek to compare the IV behavior to known leakage models.

IV. Conclusion

We have tested five different dielectric films as possible candidates for use in high temperature SiC ICs. The results of our ramped voltage testing on test capacitors fabricated from these five dielectrics indicate that silicon dioxide deposited by PECVD TEOS and silicon nitride deposited by reactive sputtering are good candidates for the intended application and merit further testing. Our test results indicate that a-SiC deposited by ion beam assisted sputtering is not adequate for use in this application and that silicon nitride deposited by PECVD also appears to be unsuitable. The three candidate dielectric materials will be further tested using thinner films to determine the optimum film for the high temperature application.

V. Acknowledgement

This work is presently funded by the NASA Aeronautics Research Mission Directorate in both the Aviation Safety and Fundamental Aeronautics Programs under the Integrated Vehicle Health Management, Subsonic Fixed Wing, and Supersonics Projects. Work was carried out by the NASA Glenn Research Center with the assistance of L. Evans, D. Lucko, K. Laster, J. Gonzalez, R. Lotenero, R. Buttler, K. Moses, M. Mrdenovich, B. Osborn, D. Androjna, A. Trunek, G. Hunter, and L. Matus. The authors thank Muthu Wijesundara (now at U.C. Davis) for deposition of a-SiC at the U.C. Berkeley Microlab.

References

- [1] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, *Proc. IEEE* 90, 1065 (2002).
- [2] F. P. McCluskey, R. Grzybowski, T. Podlesak, *High Temperature Electronics*. CRC Press, New York, 1997.
- [3] P.G. Neudeck, D. J. Spry, L.-Y. Chen, C. W. Chang, G. M. Beheim, R. S. Okojie, L. J. Evans, R. Meredith, T. Ferrier, M. J. Krasowski, and N. F. Prokop, "Long-Term Characterization of 6H-SiC Transistor Integrated Circuit Technology Operating at 500 °C," *MRS Symposium Proceedings*, vol. 1069, 2008.
- [4] P. G. Neudeck, D. J. Spry, L.-Y. Chen, G. M. Beheim, R. S. Okojie, C. W. Chang, R. D. Meredith, T. L. Ferrier, L. J. Evans, M. J. Krasowski, and N. F. Prokop, "Stable Electrical Operation of 6H-SiC JFETs and ICs for Thousands of Hours at 500 °C," to appear in *IEEE Electron Device Letters*, vol. 29, 2008.
- [5] P. G. Neudeck, D. J. Spry, L.-Y. Chen, C. W. Chang, G. M. Beheim, R. S. Okojie, L. J. Evans, R. D. Meredith, T. L. Ferrier, M. J. Krasowski, N. F. Prokop, "6H-SiC Transistor Integrated Circuits Demonstrating Prolonged Operation at 500 °C," 2008 HiTEC (Session TP1B).
- [6] D. J. Spry, P. G. Neudeck, L.-Y. Chen, G. M. Beheim, R. S. Okojie, C. W. Chang, R. D. Meredith, T. L. Ferrier, and L. J. Evans, "Fabrication and Testing of 6H-SiC JFETs for Prolonged 500 °C Operation in Air Ambient," *Proceedings of 2007 ICSCRM*, October 2007.

- [7] R. S. Okojie, D. Lukco, Y.-L. Chen, and D.J. Spry, *Journal of Applied Physics*, 91, 6553 (2002).
- [8] <http://microlab.berkeley.edu/>
- [9] <http://www.mems-exchange.org/>
- [10] A. Berman, "Time-Zero Dielectric Reliability Test by a Ramp Method," p. 204, Proc. 1981 International Reliability Physics Symposium.