

# Measurement of *n*-type dry thermally oxidized 6H-SiC metal-oxide-semiconductor diodes by quasistatic and high-frequency capacitance versus voltage and capacitance transient techniques

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Dry-oxidized *n*-type 6H-SiC metal-oxide-semiconductor capacitors are investigated using quasistatic capacitance versus voltage (*C-V*), high-frequency *C-V*, and pulsed high-frequency capacitance transient (*C-t*) analysis over the temperature range from 297 to 573 K. The quasistatic *C-V* characteristics presented are the first reported for 6H-SiC MOS capacitors, and exhibit startling nonidealities due to nonequilibrium conditions that arise from the fact that the recombination/generation process in 6H-SiC is extraordinarily slow even at the highest measurement temperature employed. The high-frequency dark *C-V* characteristics all showed deep depletion with no observable hysteresis. The recovery of the high-frequency capacitance from deep depletion to inversion was used to characterize the minority-carrier generation process as a function of temperature. Zerbst analysis conducted on the resulting *C-t* transients, which were longer than 1000 s at 573 K, showed a generation lifetime thermal activation energy of 0.49 eV.

## I. INTRODUCTION

Growing attention has recently been devoted to silicon carbide (SiC) due to its excellent material properties for high-temperature, high-power, high-frequency, and blue optoelectronics applications.<sup>1-4</sup> In addition to numerous important applications within the aerospace areas of propulsion control, power control, radar and communications, and radiation hardened circuits, a family of hostile-environment electronics would find numerous important spinoff applications in the earthbound commercial power and automobile industries. A recent theoretical appraisal<sup>2</sup> indicates that SiC power metal-oxide-semiconductor field-effect transistors (MOSFETs) and diode rectifiers would operate over higher voltage and temperature ranges, have superior switching characteristics, and yet have die sizes nearly 20 times smaller than correspondingly rated silicon-based devices. These improvements arise from the inherent material property advantages that silicon carbide enjoys over silicon, namely, a higher breakdown field (> 5 times that of Si) that permits much smaller drift regions (i.e., much lower drift region resistances), a higher thermal conductivity (> 3 times that of Si) that permits better heat dissipation, and a wide band-gap energy (2.9 eV for 6H-SiC) that enables higher junction operating temperatures.

Several crucial fabrications issues must be solved before truly advantageous SiC devices can be realized experimen-

tally. Surface passivation technology is one key area for development. Present studies focusing on SiC MOSFET technology take advantage of the fact that thermal silicon dioxide can be grown on SiC in oxygen at high temperatures.<sup>4</sup> It is obviously desirable that the SiC-SiO<sub>2</sub> interface in SiC MOSFETs mirror as closely as possible the excellent properties of the Si-SiO<sub>2</sub> interface found on high-performance silicon MOSFETs.

To closely examine the electrical properties of the dry-oxidized SiO<sub>2</sub>/6H-SiC metal-oxide-semiconductor (MOS) capacitors, we performed three different measurements. Our measurement strategy was based on corroborated reports that thermally activated, interfacial carrier generation centers are responsible for the minority-carrier generation process in wet- or dry-oxidized 6H-SiC.<sup>5-7</sup> Hence, we performed pulsed transient capacitance which is commonly known as capacitance versus time (*C-t*) measurements<sup>8,9</sup> at different temperatures to determine the activation energy of the generation process.<sup>10,11</sup> We also performed high-frequency and quasistatic capacitance versus voltage measurements<sup>12</sup> at different temperatures. Pulsed capacitance versus time measurements and high-frequency capacitance versus voltage (*C-V*) measurements have been used in the past to study SiC/SiO<sub>2</sub> interfaces.<sup>13-15</sup> To the best of our knowledge, the quasistatic *C-V* characteristics presented in this work are the first reported for 6H-SiC MOS capacitors. Our main purpose is to shed some light on the characteristics of the thermally activated generation process, to study the dry-oxidized 6H-SiC/SiO<sub>2</sub> interface more carefully, and to apply the quasistatic *C-V* method to these studies.

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## II. EXPERIMENTAL PROCEDURE AND RESULTS

### A. Sample preparation

The MOS capacitors used in our studies were formed on *n*-type nitrogen-doped 6H-SiC epitaxial layers grown by chemical-vapor deposition<sup>16</sup> onto a commercially available<sup>17</sup> 6H (0001) silicon-face SiC substrate polished 3° off the basal plane. The epitaxial layer thickness was approximately 8 μm with an *n*-type carrier concentration of  $2 \times 10^{16} \text{ cm}^{-3}$  ascertained from the *C-V* measurements reported herein. Immediately following epitaxial growth, the samples were transferred to a horizontal hot-wall quartz tube furnace with no intermediate cleaning steps, and a 7 h 1150 °C oxidation was performed under a pure oxygen flow of 0.5 scfm that resulted in a 495-Å-thick oxide. During oxidation, the samples sat horizontally on a quartz susceptor, and push/pull times of 2 min were employed. Following oxidation, circular and square aluminum contacts (areas  $\leq 4 \times 10^{-4} \text{ cm}^2$ ) were deposited onto the wafer by thermal evaporation and patterned by liftoff. The contact mask included a die border grid which spanned the wafer's top surface and acted as a large-area substrate contact during electrical testing.

### B. Electrical measurement procedures

The 6H-SiC MOS capacitors were characterized by both the high-frequency (1 MHz) *C-V* and the quasistatic *C-V* at temperatures from 295 up to 573 K. Except in a few cases, the high-frequency *C-V* sweep rate of 1 V/s was chosen with sweep voltage parameters from -20 to 10 V or from 10 to -20 V. In the case of the quasistatic *C-V* measurement, identical sweep voltage parameters were used with a slower sweep rate of 100 mV/s to prevent erroneous quasistatic *C-V* characteristics.<sup>12</sup>

The *C-V* measurements were performed using Keithley model 590 (high-frequency *C-V* meter at 1 MHz) and Keithley model 595 (quasistatic *C-V* meter) instruments. The pulsed capacitance versus time measurements were performed using the high-frequency meter with a computer-controlled acquisition system that performed triggering, voltage pulse control, and data acquisition. Except where noted, the *C-V* measurements were carried out in the dark.

### C. High-frequency *C-V* measurements

Typical high-frequency *C-V* traces are shown in Fig. 1. At all temperatures the characteristics were swept in both directions, but no appreciable hysteresis was observed under dark conditions. The high-frequency *C-V* shows deep depletion for negative gate voltages at temperatures as high as 573 K. In the inset of Fig. 1, the temperature dependence of the flatband voltage is shown. The flatband voltage increased from 0.75 V at 300 K to 1.6 V at 473 K. It is well known, however, that slow traps and slow minority-carrier generation processes are unable to respond to the ac test signal of the high-frequency *C-V* measurement.<sup>12</sup>

In Fig. 1 we have also included traces that show the behavior of the *C-V* when the device was illuminated with ultraviolet light from a mercury arc lamp. UV illumination results in inversion capacitance characteristics, hysteresis in

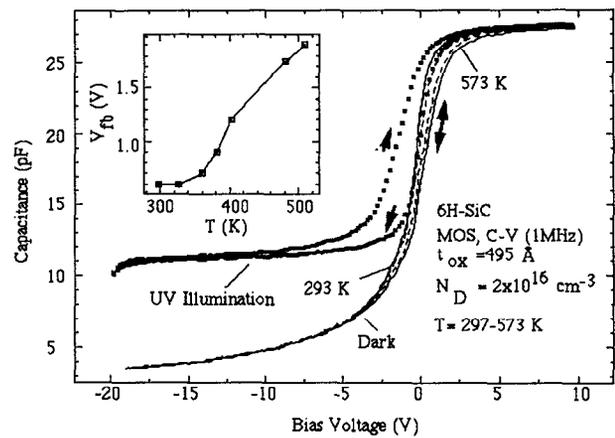


FIG. 1. High-frequency capacitance vs voltage measurements at different temperatures. Sweeps were carried out in both directions with no appreciable hysteresis in the dark. The inset shows the flatband voltage as a function of temperature.

the *C-V* traces, and a shift of the flatband voltage to less positive values. It is interesting to note that the UV light and temperature affect the charges responsible for the flat band voltage in the opposite manner. We note that temperature and illumination can be used to alter the value of the flatband voltage, and hence the charges appear to reside in slow interface traps as opposed to being fixed oxide charges. We also note that these slow traps can be filled by increasing temperature or they can be emptied by illumination.

### D. Capacitance transient measurements

Next we pulsed the gate voltage of our MOS devices from positive 10 V (accumulation) to negative 10 V (deep depletion) and monitored the transient high-frequency capacitance as a function of time. The results are shown in Fig. 2. Using a well-established procedure,<sup>9,12</sup> we constructed Zerbst plots using capacitance-transient (*C-t*) traces of Fig. 2 and calculated the generation lifetime as a function of temperature. A typical Zerbst plot at 548 K is shown in Fig. 3.

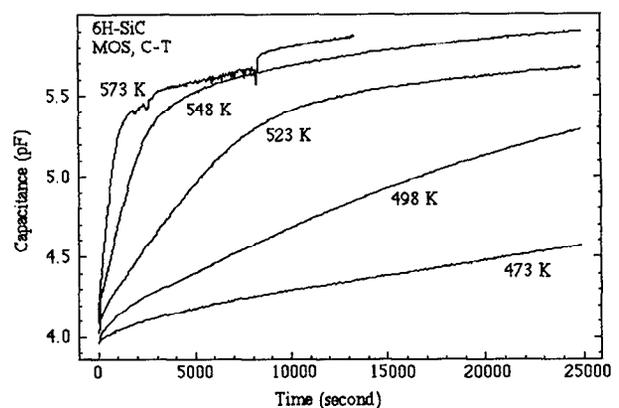


FIG. 2. Transient capacitance vs time measurements at temperatures ranging from 473 to 573 K. The gate bias was switched from +10 to -10 V at time  $t=0$ .

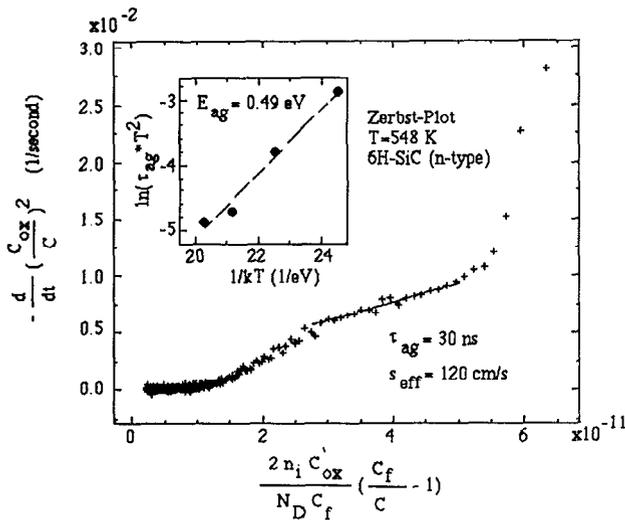


FIG. 3. Zerbst plot constructed using the  $T=548$  K  $C-t$  trace shown in Fig. 2. Using Zerbst plots constructed from the  $C-t$  traces at different temperatures, the generation lifetime as a function of temperature was calculated resulting in the Arrhenius plot shown in the inset.

Zerbst plots at different temperatures are similar to the one shown in this figure. In calculating the slope, we only used the middle part of the Zerbst plots where it is relatively linear. We noted that Zerbst plots have very narrow linear regions followed by classical shapes near the origin (corresponding to the final stages of  $C-t$  traces) and at large values of abscissa (corresponding to the initial stages of  $C-t$  traces). The carrier generation process is thermally activated, and in our samples its activation process was  $0.49$  eV as shown in Fig. 3 inset.

### E. Quasistatic C-V measurements

Figure 4 shows quasistatic  $C-V$  traces corresponding to measurements that were performed at five different temperatures. Our studies did not show any differences between the high-frequency and quasistatic  $C-V$  characteristics with various sweep rates at room temperature. Both the high-

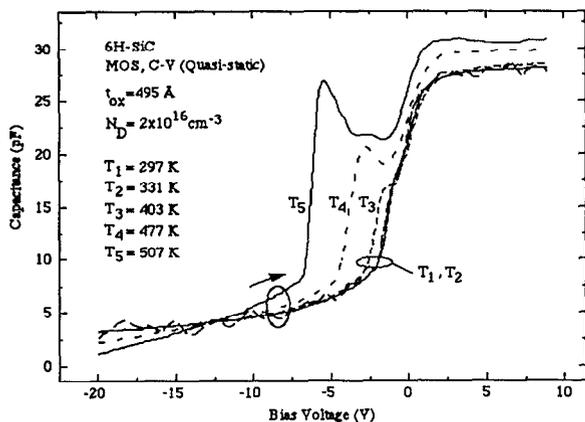


FIG. 4. Quasistatic capacitance vs voltage curves at five different temperatures for sweeps from  $-20$  to  $+10$  V at a constant rate of  $100$  mV/s.

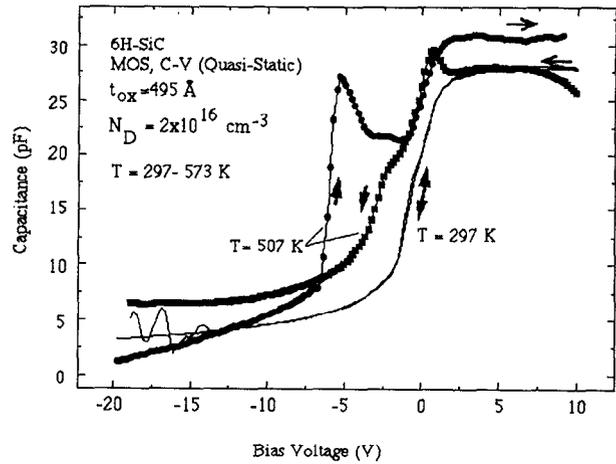


FIG. 5. Quasistatic capacitance vs voltage curves at room temperature and  $507$  K showing sweeps carried out in both sweep directions at a sweep rate of  $100$  mV/s.

frequency and quasistatic  $C-V$  measurements exhibit almost identical curves at room temperature with no inversion layer observed due to lack of minority carriers consistent with the fact that  $6H-SiC$  is a wide band-gap material with extremely low minority-carrier generation rates. As the temperature is increased above  $400$  K, however, a large peak becomes increasingly prominent in the quasistatic  $C-V$  traces at gate voltages corresponding to depletion/deep-depletion of the semiconductor surface. Figure 5 shows that the height of the peak in the quasistatic  $C-V$  depends on the sweep direction and is most pronounced when the gate voltage is swept from deep depletion toward accumulation. Moreover, Fig. 6 shows that the height of the peak also increased as we stressed at a gate bias of  $-20$  V for longer periods of time. Although not shown here, the height of the peak decreased dramatically when we stressed the device under positive gate voltages immediately prior to a sweep from  $-20$  to  $+10$  V, or as shown in Fig. 5 when the sweep direction was from positive

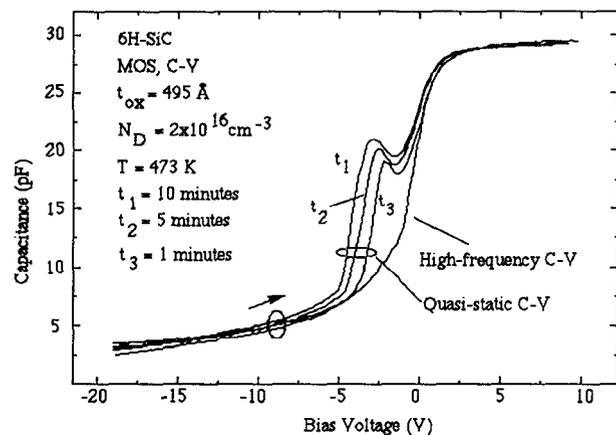


FIG. 6. Quasistatic capacitance vs voltage curves as a function of stress duration at  $-20$  V immediately prior to sweeping from  $-20$  to  $+10$  V at  $473$  K. Stress times of  $1$ ,  $5$ , and  $10$  min were employed. It was separately verified that the gate voltage did not momentarily deviate from  $-20$  V between the end of the stress period and the beginning of the  $-20$  to  $+10$  V sweep.

to negative gate voltages. Using sequential bias stress tests we observed that the peak in the quasistatic  $C$ - $V$  can be made larger or smaller in a reversible manner depending on the stress conditions and sweep polarity as discussed above.

We note there is an increase in the accumulation capacitance as a function of temperature. This reduction mathematically corresponds to a 5 Å effective reduction in the thickness of the oxide layer at high temperatures, which may be possible considering that some previous work<sup>18,19</sup> has suggested that the 6H-SiC/SiO<sub>2</sub> interface is less abrupt than the Si/SiO<sub>2</sub> interface. Another possible mechanism that may be responsible for this observed increase of quasistatic accumulation capacitance at high temperatures is the presence of thermally activated mobile charges at the surface of the oxide. Since we have both of our measurement electrodes are on the surface of the sample, mobile surface charges can provide a leakage path increasing the measured capacitance. For more discussion on the contribution of these charges to the measured quasistatic capacitance of SiO<sub>2</sub>/Si MOS capacitors, Ref. 12 should be consulted.

### III. DISCUSSION

The most striking feature of all the measurements collected in this work is the large peak observed in the depletion/deep-depletion regime of the quasistatic measurements presented in Figs. 4–6. This peak cannot be attributed to mobile sodium ion contamination of the oxide for two reasons:<sup>12,20</sup> First, the high-frequency  $C$ - $V$  characteristics in the dark (Fig. 1) exhibit no appreciable hysteresis even at temperatures as high as 573 K; second, the voltage and sweep direction at which the large peak occurs is inconsistent with the motion of Na<sup>+</sup> under the oxide electric field present at the applied gate voltages.

Instead, we believe that this peak is a most interesting 6H-SiC manifestation of the nonequilibrium quasistatic effects observed at low temperatures in silicon MOS capacitors by Kuhn and Nicollian.<sup>21</sup> Kuhn and Nicollian attributed their silicon quasistatic peaks, some of which are very similar in appearance and behavior to the 6H-SiC quasistatic peaks in Figs. 4 and 5, to the injection of excess minority-carrier surface charge into the substrate which occurs at low temperatures when the surface charge does not recombine fast enough to maintain equilibrium with the sweep out of partial inversion toward accumulation. Owing to the wide band gap and extraordinarily slow minority-carrier recombination/generation process in 6H-SiC relative to silicon, we propose that we are observing an entirely analogous phenomena occurring in the  $T = 400$ – $600$  K temperature range for 6H-SiC as occurs in the quasistatic measurement of silicon MOS capacitors around the  $T = 100$ – $200$  K temperature range.

The detailed physics and modeling of this phenomenon in wide-band-gap semiconductors will be the subject of a subsequent article.<sup>22</sup> However, we wish at this time to point out that the nonequilibrium excess surface charge behind this phenomena is actually the sum of inversion layer charge and surface state charge.<sup>21</sup> The fact that the peak rises almost up to the accumulation capacitance at 507 K in Fig. 4, coupled with the relative lack of interface state stretch-out in Fig. 1, indicates that inversion layer charge is dominant at the high-

est temperatures measured in this work. However, one cannot rule out the possibility that slow trapped surface state charge may be playing a significant role in the quasistatic characteristics, particularly in the flatter ledges and small bumps observed between accumulation and the onset of partial inversion.

The behavior of the large peak in each part of Figs. 4–6 is entirely consistent with the expected behavior of the surface charge as a function of temperature (Fig. 4), sweep direction (Fig. 5), and deep-depletion stress time (Fig. 6). As the temperature is increased, one would expect increased thermal generation to more rapidly buildup inversion charge leading to the behavior observed in Fig. 4. In Fig. 5, the high-temperature sweep from accumulation to deep depletion does not instantly generate an appreciable number of excess minority surface charges, nor would that sweep direction lead to the injection of excess minority carriers into the substrate. As the deep-depletion stress time is increased, a larger minority-carrier charge is accumulated leading to the monotonically increasing peak sizes displayed in Fig. 6.

The activation energy associated with the generation process  $E_{ag}$ , calculated using Zerbst plots at different temperatures and the Arrhenius plot shown in the Fig. 3 inset, is 0.49 eV in these dry-oxidized MOS samples. The temperature dependence of  $\tau_{ag}$  can be related to the generation rate  $G$  by<sup>8</sup>

$$G = n_i / \tau_{ag}. \quad (1)$$

The intrinsic carrier concentration  $n_i$  in Eq. (1) has a thermal activation energy very close to  $-E_G/2 \approx -1.5$  eV.<sup>23,24</sup> Because both terms in Eq. (1) are thermally activated processes, the temperature dependence of Eq. (1) is also thermally activated with a corresponding generation activation energy  $E_{AG}$  of

$$E_{AG} = -E_G/2 - E_{ag}. \quad (2)$$

Using Eq. (2) we find that our  $\tau_{ag}$  activation energy of 0.49 eV is very comparable to the generation rate activation energy  $E_{AG} = -2$  eV observed by others working on nearly identical  $n$ -type dry-oxidized 6H-SiC MOS capacitors produced and measured elsewhere.<sup>7</sup>

The presence of electron traps in SiO<sub>2</sub> is well established during the past 15 years. These traps have been shown to be neutral, and upon trapping electrons they become negatively charged. In wet-oxidized silicon MOS samples, the trapping of electrons by these acceptor-like traps initiates a chemical reaction that consumes the water-related traps, thereby reducing trapping events. Although our samples were dry oxidized, the behavior is consistent with the presence of acceptor-like traps and that their electron occupancy was increased by increasing the temperature (from  $3.3 \times 10^{11}$  cm<sup>-2</sup> at 300 K to  $6.8 \times 10^{11}$  cm<sup>-2</sup> at 473 K calculated using the flatband voltage shift shown in the Fig. 1 inset). Moreover, the electron occupancy of these traps appears to be reduced by UV illumination (shown in Fig. 1).

To further investigate interface states, we considered two well-established methods:<sup>12</sup> (i) the Terman method, and (ii) the so-called high-low method. In the Terman method one compares an experimental high-frequency  $C$ - $V$  trace with its

theoretical counterpart and any deviation of the experimental trace from the theoretical trace is attributed to the presence of the interface traps. It is well known that the Terman method has many shortcomings, including the fact that it is unable to yield any information regarding very slow (presumably deep) traps with response times that are long compared to the  $C$ - $V$  sweep time.<sup>12</sup> As the measurement temperature is increased, however, a larger number of the slow traps should be thermally excited to respond to the sweep. This behavior was in fact observed, as the Terman method extracted trap densities from the high-frequency  $C$ - $V$  characteristics (Fig. 1) of around  $2 \times 10^{11}/\text{cm}^2 \text{ eV}$  at room temperature, increasing to approximately  $8 \times 10^{11}/\text{cm}^2 \text{ eV}$  at 573 K.

The high-low method extracts the interface trap densities by comparing the high-frequency and quasistatic (i.e., low-frequency)  $C$ - $V$  traces. In the case of the quasistatic  $C$ - $V$  measurements, some slower interface traps are able to respond to the quasistatic measurement signal. In the ideal case where the interface traps and minority carriers are at equilibrium with the dc gate voltage in both high- $f$  and quasistatic measurements, the only differences that these two measurements have are the contribution of the interface traps and the minority carriers to the quasistatic capacitance. However, in our 6H-SiC measurements the minority carriers and interface traps are clearly not in equilibrium with the gate dc voltage and the quasistatic capacitance signal, even at temperatures as high as 573 K.

In Ref. 21 Kuhn and Nicollian state that nonideal peaks and ledges could appear in the quasistatic characteristics of totally ideal surface-state-free MOS capacitors due solely to the nonequilibrium discharge of the inversion layer. This assertion would appear to cast doubt on the use of the high-low technique in the nonequilibrium case when sweeping from inversion toward accumulation, since differences between the ideal and measured low- $f$  characteristics due purely to nonequilibrium effects could be mistakenly calculated (using the high-low method) into artificially high interface-state densities.<sup>12</sup> When sweeping from accumulation toward deep depletion, incomplete inversion layer formation could also lead the high-low method to calculate misleading interface-state densities. Given these concerns, it is the authors' opinion that direct application of the high-low calculation to the high- $f$  and quasistatic  $C$ - $V$  data may not yield meaningful and reliable interface state data. We are presently undertaking an in-depth study of nonequilibrium quasistatic measurements in wide-band-gap semiconductors to further resolve this important issue.<sup>22</sup>

#### IV. CONCLUSION

In summary, the quasistatic  $C$ - $V$  approach has been incorporated into the characterization of the 6H-SiC/SiO<sub>2</sub> MOS capacitors for the first time. The quasistatic characteristics exhibited startling nonidealities due to nonequilibrium conditions that arise due to the extraordinarily slow recombination/generation process in 6H-SiC. These nonidealities, which were mainly in the form of peaks and ledges exhibited at temperatures above 473 K, appear to preclude the straightforward calculation of reliable interface state densities via the high-low methodology. The high-frequency

dark  $C$ - $V$  characteristics all showed deep depletion with no observable hysteresis. Apparent interface-state densities extracted from the high-frequency  $C$ - $V$  characteristics via the Terman technique increased from  $\sim 2 \times 10^{11}/\text{cm}^2 \text{ eV}$  at 24 °C to  $\sim 8 \times 10^{11}/\text{cm}^2$  at 573 K, which supports the argument that a greater number of slow (presumably deep) traps are able to respond to  $C$ - $V$  sweeps at higher temperatures. The recovery of the dark high-frequency capacitance from deep depletion was used to characterize inversion layer formation through minority-carrier generation as a function of temperature. Zerst analysis conducted on the resulting  $C$ - $t$  transients revealed a generation lifetime activation energy of 0.49 eV, which is consistent with generation rate behavior reported by others on dry-oxidized  $n$ -type MOS 6H-SiC capacitors.

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